CLAIMS

1. A method of forming a field-effect transistor on a substrate, said method comprising steps of:

forming a buffer layer on said substrate, said buffer layer comprising ALD silicon dioxide;

forming a high-k dielectric layer over said buffer layer.

2. The method of claim 1 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

3. The method of claim 1 wherein said step of forming said buffer layer comprises utilizing a silicon tetrachloride precursor in an atomic layer deposition process.

4. The method of claim 1 wherein said buffer layer comprises substantially no pin-hole defects.

5. The method of claim 1 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

6. The method of claim 2 wherein said gate electrode layer comprises polycrystalline silicon.

7. The method of claim 1 wherein said high-k dielectric layer is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

8. A method for forming a field effect transistor on a substrate, said method comprising a step of forming a buffer layer on said substrate, said method being characterized by:

forming a high-k dielectric layer on said buffer layer, wherein said buffer layer comprises ALD silicon dioxide.

9. The method of claim 8 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

10. The method of claim 8 wherein said step of forming said buffer layer comprises utilizing a silicon tetrachloride precursor in an atomic layer deposition process.

11. The method of claim 8 wherein said buffer layer comprises substantially no pin-hole defects.

12. The method of claim 8 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

13. The method of claim 9 wherein said gate electrode layer comprises polycrystalline silicon.

14. The method of claim 8 wherein said high-k dielectric layer is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

15. A field effect transistor situated on a substrate, said field effect transistor comprising:

a buffer layer situated on a substrate, said buffer layer comprising ALD silicon dioxide;

a high-k dielectric layer situated on said buffer layer;

a gate electrode layer situated on said high-k dielectric layer.

16. The field effect transistor of claim 15 wherein said buffer layer comprises substantially no pin-hole defects.

17. The field effect transistor of claim 15 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

18. The field effect transistor of claim 15 wherein said buffer layer has a uniform thickness on said substrate.

19. The field effect transistor of claim 15 wherein said gate electrode layer comprises polycrystalline silicon.

20. The field effect transistor of claim 15 wherein said high-k dielectric layer is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.